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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,195	12/21/2000	Toshiyuki Hirota	040373/0300	7014

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EXAMINER
VU, QUANG D

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,195	HIROTA ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 04/21/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9,11-16,18-23 and 25-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9,11-16,18-23 and 25-28* is/are rejected.

7)☒ Claim(s) *29-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Objections

Claims 1, 6, 11 and 18 are objected to because of the following informalities: Claim 1, lines 17-18 and 27-28 (or claim 6, lines 18-19 and 28-29; or claim 11, lines 19-20 and 29-30; or claim 18, lines 19-20 and 29-30), the phrase "annealing an assembly..." fails to clarify what is an assembly. Appropriate correction is required.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-4, 6-9, 18-23, 25, 26, 28, 29, 30 and 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 lines 13-14, (or claim 6, in lines 14-15; or claim 18, lines 15-16), the phrase "uniformly forming a second nitride film having a predetermined thickness on the surface on which the first nitride film is etched" fails to reflect the subject matter of the instant invention, in which the second nitride film is not only formed on the first nitride film which is etched at the low density region (103), but also formed on the first nitride film at the high density region (102).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 11-16, 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of US Patent No. 6,326,270 to Lee et al.

AAPA (figures 1-7) teach a method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region (cell array region) containing transistor elements arrayed at a high density and a low-density region (peripheral circuit region) containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film (115) on a surface of the semiconductor substrate (101);

forming gate electrodes (116) on a surface of the gate oxide film (115), and forming oxide film (119) on the gate electrodes (116);

uniformly forming a first nitride film (131) having a predetermined thickness on the surface with the gate electrodes (116) formed thereon;

masking the high density region of the semiconductor substrate (101), and etching the first nitride film (131) in only the low density region to expose the gate oxide film (115) in gaps between the gate electrodes (116);

forming contact electrodes (122) connected to the semiconductor substrate (101) in the contact holes (121).

AAPA differs from the claimed invention by not showing annealing an assembly formed so far in an atmosphere containing water vapor; and annealing an assembly formed so far with a forming gas to recover an interfacial level. Such a step of annealing is well known in the art as shown for example by US Patent No. 5,930,584 to Sun et al. (column 3, lines 13-21). It would have been obvious to one having ordinary skill in the art at the time the invention was made for annealing an assembly formed so far in an atmosphere containing water vapor, since it is common in the art to perform annealing steps to repair substrate damage, activate dopants, form silicide and other reasons. Additionally, it is also well known in the art to perform annealing steps at different times during fabrication.

AAPA differs from the claimed invention by not showing uniformly forming a second nitride film having a predetermined thickness on the surface on which the first nitride film is etched. However, Lee et al. (figure 3A-G, 5) teach uniformly forming a second nitride film (119) having a predetermined thickness on the surface on which the first nitride film (112) is etched. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate to form a second nitride film of Lee et al. into the device taught by Admitted Prior Art because it protects the gate electrode against over etching.

The combined device shows that forming an interlayer insulating film (133) on the second nitride (119) with an impurity introduced therein on a surface of the second nitride film.

The combined device shows that self-aligning the high-density region using the first nitride film (131) positioned on sides of the gate electrodes (116) as an etching stopper to form contact holes (122) reaching the semiconductor substrate (101) in the interlayer insulating film (133), wherein portions of the second nitride film (119) that are in direct contact with the first

nitride film (112) and that are positioned on at least one of the respective sides of the gate electrodes (116) are removed as a result of the self aligning step.

Regarding claims 2 and 12, AAPA and Lee et al. differ from the claimed invention by not showing the first nitride film and the second nitride film is formed by a CVD. AAPA and Lee et al. are silent with respect to how the nitride film is deposited. One having ordinary skill in the art would have been required to select a known method of deposition. It would have been obvious to select CVD, since it is a well-known method.

Regarding claims 3 and 13, AAPA and Lee et al. do not teach a method, wherein the first nitride film is formed to a thickness ranging from 30 to 50 nm. Lee et al. teach a method, wherein the thickness of the first and second nitride films are formed to a thickness of about 20 – 200 Angstroms (2-20 nm) (column 8, lines 1-3) and 50-150 Angstroms (5-15nm) (column 9, lines 37-38), respectively. Lee et al. teach a method, wherein the second nitride film is formed to a thickness ranging from 3.0 to 20 nm. It would have been obvious to one having ordinary skill in the art at the time of the invention was made for the first nitride film is formed to a thickness ranging from 30 to 50 nm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 4 and 16, AAPA and Lee et al. teach a method, wherein the first nitride film is formed to a thickness large enough to serve as an etching stopper for self-aligning the high-density region.

It is inherent that the second nitride film is formed to a thickness which prevents an impurity of the interlayer insulating film from being diffused into the semiconductor substrate by

annealing the assembly in the atmosphere containing the water vapor and also prevents the semiconductor substrate from being oxidized by annealing the assembly in the atmosphere containing the water vapor, but allow the forming gas to be diffused into the semiconductor substrate. They are known in the art as shown for example by JP02-87622, US Patent No. 5,116,768 to Kawamura (column 3, lines 25-31), and US Patent No. 4,927,770 to Swanson (abstract, lines 3-5).

Regarding claim 11, the disclosures of AAPA and Lee et al. are discussed as applied to claim 1, AAPA further teaches etching the first nitride film (131) and gate oxide film (115) to expose the substrate (101) in gaps between gate electrodes (116) in the low-density region.

Regarding claim 14, AAPA and Lee et al. do not teach a method, wherein the first nitride film is formed by a chemical vapor deposition process, and the second nitride film is formed by a rapid thermal nitriding process. AAPA and Lee et al. is silent with respect to how the first nitride film is deposited. It would have been obvious to select CVD, since it is a well-known method. Rapid thermal nitriding is a well known a method of forming nitride layer. It would have been obvious to select rapid thermal nitriding, since it is a well-known method.

Regarding claim 15, AAPA and Lee et al. differ from the claimed invention by not showing a method, wherein the first nitride film is formed to a thickness ranging from 30 to 50 nm. Lee et al. teach a method, wherein the second nitride film is formed to a thickness of 2.0 nm (20 Angstroms; column 8, lines 1-3). It would have been obvious to one having ordinary skill in the art at the time of the invention was made for the first nitride film is formed to a thickness ranging from 30 to 50 nm, since it has been held that where the general conditions of a claim are

disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 25 and 27, the combined device shows that a method, wherein the second nitride film only remains directly beneath the interlayer insulating film after the self-aligning step is completed.

5. Claims 6-9, 18-23, 26, 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lee et al. as applied to claims 1-4 above, and further in view of US Patent No. 5,807,779 to Liaw.

The disclosures of AAPA and Lee et al. are discussed as applied to claim 1, AAPA further differs from the claimed invention by not showing to form the nitride protective film on the gate electrodes. However, Lee et al. (figures 3A-G, 5) teach to form the nitride protective film (106) on the gate electrodes. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the nitride protective film on the gate electrodes, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

The combined device (AAPA and Lee et al.) differs from the claimed invention by not showing to expose the nitride protective films on the gate electrodes. However, Liaw (figure 2) teaches to expose the nitride protective films (5) on the gate electrodes. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Liaw into the device taught by Lee et al. because it uses to form contact hole on the gate electrode.

Regarding claim 18, the disclosures of AAPA and Lee et al. are discussed as applied to claim 6, AAPA further teaches etching the first nitride film (131) and gate oxide film (115) to expose the substrate (101) in gaps between gate electrodes (116) in the low-density region.

Regarding claim 21, AAPA and Lee et al. do not teach a method, wherein the first nitride film is formed by a chemical vapor deposition process, and the second nitride film is formed by a rapid thermal nitriding process. AAPA and Lee et al. are silent with respect to how the first nitride film is deposited. It would have been obvious to select CVD, since it is a well-known method. Rapid thermal nitriding is a well known a method of forming nitride layer. It would have been obvious to select rapid thermal nitriding, since it is a well-known method.

Regarding claim 22, AAPA and Lee et al. do not teach a method, wherein the first nitride film is formed to a thickness ranging from 30 to 50 nm, and the second nitride film is formed to a thickness ranging from 1.8 to 2.0 nm. Lee et al. teach a method, wherein the thickness of the first and second nitride films are formed to a thickness of about 20 –200 Angstroms (2-20 nm) (column 8, lines 1-3) and 50-150 Angstroms (5-15nm) (column 9, lines 37-38), respectively. It would have been obvious to one having ordinary skill in the art at the time of the invention was made for the first nitride film is formed to a thickness ranging from 30 to 50 nm, and the second nitride film is formed to a thickness ranging from 1.8 to 2.0 nm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 26 and 28, the combined device shows that a method, wherein the second nitride film only remains directly beneath the interlayer insulating film after the self-aligning step is completed.

Allowable Subject Matter

6. Claims 29, 30, 31 and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: The prior art, including the most closely related art, AAPA, US Patent No. 6,326,270 to Lee et al. and US Patent No. 5,807,779 to Liaw, does not anticipate or render obvious a method of manufacturing a semiconductor device as defined in the above allowed claims, comprising particularly: planarizing a top surface of the interlayer insulating film, wherein the step of self-aligning the high-density region comprises the steps of forming an oxide film on the panelized top surface of the interlayer insulating film; and in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist, wherein the step of planarizing is performed after the step of annealing in an atmosphere containing water vapor and before the step of self-aligning the high density region.

Response to Arguments

8. Applicant's arguments with respect to claims 1-4, 6-9, 11-16, 18-23 and 25-32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
July 23, 2003

SHOUXIANG HU
PRIMARY EXAMINER